UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/612,260	07/07/2000	Guy M. Cohen	YOR9-2000-0174	7116

28211 7590 09/25/2003

FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER
KANG, DONGHEE

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/612,260	COHEN ET AL.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20,44,47,48,50,51 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *44* is/are allowed.

6)☒ Claim(s) *1-20,47,48,50,51 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Acknowledgment

1. Claims 45,46, 49, 52 & 54 have been cancelled. Thus claims 1-20, 44, 47-48, 50-51 & 53 are pending in this application.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 20 December 2002 has been entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **1, 4, 7-10, & 47** are rejected under 35 U.S.C. 102(b) as being anticipated by Yamanaka (US 5,834,797).

Regarding claim **1**, Yamanaka teaches a transistor comprising (Figs.8A & 8B): a channel region (4); a first gate (G2) on top of said channel region; a second gate (G1) below said channel region; and an isolation layer (3) below said second gate

(G1), wherein said first gate (G2) and said second gate are aligned and electrically separated from each other,

wherein a material composition of said second gate is independent of a material composition of said isolation layer.

Although Yamanaka does not teach the first and second gates are self-aligned, the "self-aligned" is a product-by-process limitation. The product-by-process claims are given no patentable weight. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production.

If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process". In re Thorpe, 777F. 2d 695,698 USPQ 964, 966 (Fed. Cir.1985). See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claim **4**, Yamanaka teaches the transistor further comprising a first gate dielectric (51&52) below said first gate (G2) and a second gate dielectric (30) above said second gate.

Regarding claim **7**, Yamanaka teaches the first gate comprising a different thickness than said second gate.

Regarding claim **8**, Yamanaka teaches said first gate, said second gate and said channel region form a planarized structure.

Regarding claim **9**, Yamanaka teaches said first gate dielectric comprises a different material than said second gate dielectric.

Regarding claim **10**, Yamanaka teaches said first gate dielectric comprises a different thickness than second gate dielectric.

Regarding claim **47**, Yamanaka teaches the transistor further comprising:

Source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and source and drain dielectric between said source and drain regions and said first gate and said second gate,

Wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectric.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **2-3 & 53** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka.

Regarding claims **2-3**, Yamanaka teaches substantially the entire claimed structure, applied to claim 1 as explained above, except that the first gate comprising a different doping concentration and doping species than said second gate. It is, however, conventional in the art to select the concentration of gate electrode to adjust a threshold voltage in the transistor. If the first gate electrode has a lower concentration than the

second gate electrode, a threshold voltage of the first gate is lower than that of the second gate. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed Yamanaka's "first and second gate" having a different concentration, since the different concentration of gate electrode provides the different threshold voltage in device.

Regarding claim **53**, Yamanaka teaches the channel region formed in silicon substrate. Although Yamanaka does not expressly teach the silicon substrate is single crystalline silicon. It is conventional in the art the single crystalline silicon used as a substrate. Therefore, it would have been obvious to one of ordinary skill in the art to use the single crystalline silicon for substrate material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as matter of obvious design choice. In re Leshin, 125 USPQ 416.

7. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Uesugi et al. (US 5,708,286).

Yamanaka applies to claim 1 above.

Yamanaka fails to teach the first conductive contact of first gate and second conductive contact of second gate are coplanar. However, Uesugi teaches in Fig.1 & Col.7, lines 42-46 the first conductive contact (80) of first gate (60) and second conductive contact (90) of second gate (30) are coplanar. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine

the teaching of Uesugi with Yamanaka's device in order to reduce the manufacturing process.

8. Claims **6, 11-16, 18-20, 48, 50-51** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Pfiester (US 5,166,084).

Regarding claims **6 & 11**, Yamanaka teaches a semiconductor chip having at least one transistor, said transistor comprising (Figs. 8a & 8b);

a channel region (4); a first gate (G2) on top of said channel region; a second gate (G1) below said channel region; and an isolation layer (3) below said second gate (Col.12, line 41-Col.14,line 4).

Although Yamanaka does not teach the first and second gates are self-aligned, the "self-aligned" is a product-by-process limitation. The product-by-process claims are given no patentable weight.

Yamanaka does not teach the first gate comprising a different material than said second gate. However, Pfiester teaches in Fig.4 the first gate electrode (24) comprising a different material than said second gate electrode (26). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Pfiester into Yamanaka's device, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for intended use as a mater of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims **12-13**, neither Yamanaka nor Pfiester teaches the first gate comprising a different doping concentration and doping species than said second gate. It is, however, conventional in the art to select the concentration of gate electrode to adjust a threshold voltage in the transistor. If the first gate electrode has a lower concentration than the second gate electrode, a threshold voltage of the first gate is lower than that of the second gate. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed Yamanaka's "first and second gate" having a different concentration, since the different concentration of gate electrode provides the different threshold voltage in device.

Regarding claim **14**, Yamanaka as modified by Pfiester teaches the transistor further comprising a first gate dielectric (51 & 52) below said first gate (G2) and a second gate dielectric (30) above said second gate (G1).

Regarding claim **15**, Yamanaka as modified by Pfiester teaches said first gate dielectric (30) comprises a different material than said second gate dielectric.

Regarding claim **16**, Yamanaka as modified by Pfiester teaches said first gate dielectric comprising a different thickness than second gate dielectric.

Regarding claim **18**, Yamanaka as modified by Pfiester teaches said first gate and said second gate are electrically separated.

Regarding claim **19**, Yamanaka as modified by Pfiester teaches the first gate and said second gate having a different thickness.

Regarding claim **20**, Yamanaka as modified by Pfiester teaches said first gate, said second gate and said channel region form a planarized structure.

Regarding claim **48**, Yamanaka as modified by Pfiester teaches the semiconductor chip further comprising source and drain regions laterally adjacent said channel region, wherein said source and drain regions do not horizontally overlap said first or said second gate. Although Yamanaka does not teach the first and second gates are self-aligned, the "self-aligned" is a product-by-process limitation. The product-by-process claims are given no patentable weight.

Regarding claim **50**, Yamanaka as modified by Pfiester teaches the semiconductor chip further comprising source and drain regions laterally adjacent said channel region, said first gate and said second gate.

Regarding claim **51**, Yamanaka as modified by Pfiester teaches the transistor further comprising:

source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and source and drain dielectric between said source and drain regions and said first gate and said second gate,

wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.

9. Claim **17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka in view of Pfiester and further in view of Uesugi et al. (US 5,708,286).

Yamanaka as modified by Pfiester applies to claim 11 above.

Neither Yamanaka nor Pfiester teaches the first conductive contact of first gate and second conductive contact of second gate are coplanar. However, Uesugi teaches

in Fig.1 & Col.7, lines 42-46 the first conductive contact (80) of first gate (60) and second conductive contact (90) of second gate (30) are coplanar. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Uesugi with Yamanaka's device in order to reduce the manufacturing process.

Allowable Subject Matter

10. Claim **44** is allowed.

The following is an examiner's statement of reasons for allowance:

Prior art reference, taken along or in combination, do not teach or render obvious that the channel region includes an extension into the source and drain regions.

Response to Arguments

11. Applicant's arguments filed 20 December 2002 have been fully considered but they are not persuasive. Yamanaka teaches a material composition of said second gate is independent of a material composition of said isolation layer.

Claim 45 has been cancelled in Paper No.19 received on 19 November 2002.

Claim 44 is allowed.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang

dhk
March 21, 2003